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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,615	10/28/2003	Se-Jin Ahn	5649-1202	6846

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EXAMINER	
CRANE, SARA W	
ART UNIT	**PAPER NUMBER**
2811	
MAIL DATE	**DELIVERY MODE**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/696,615	AHN ET AL.	
	Examiner	Art Unit	
	Sara W. Crane	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,38-40 and 45-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,38-40 and 45-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-11 and 48-53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 and claim 48 each now recite a word line crossing over the data line and covering both sidewalls of the multi-junction storage pattern. It is not clear what is meant by "sidewalls of the multi-junction storage pattern." Reference to the sidewalls is made without any explicit antecedent. Sometimes the word sidewall means simply the vertical side wall of the structure. Sometimes the word sidewall refers to an insulating layer that is located at the vertical side wall of the structure. It is not clear which meaning is intended here. Applicant's invention does in fact include such an insulating layer at each vertical side wall of structure overlying the part of the channel labeled "L1," so claims 2 and 48 may mean that there are insulating "sidewalls" which are "covered by" (or in contact with) the word line. If the claims are not intended to encompass insulating structures at the side vertical walls of the multi-junction storage pattern, then it is not clear what is meant by "covering." At any rate, the scope of claim coverage is not clear.

Claim 48 refers to the sidewalls "of the multi-junction storage pattern." There is no antecedent for "the multi-junction storage pattern."

Claim Rejections - 35 USC § 103

Claims 1, 12, 38-40, 45-47, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato et al. in view of Hori.

See reasons of record in the Office action of 15 November 2006.

Allowable Subject Matter

Claims 2 and 48, and claims depending from claims 2 and 48, would be allowable if expressed in completed form, including all of the limitations of the base claims, and if the meaning of the claim language related to covering of sidewalls of a multi-junction storage pattern is clarified, as discussed above in the rejection under 35 U.S.C. 112, second paragraph.

Conclusion

Applicant's arguments presented with respect to the rejected claims have been considered, but are not convincing. Applicant argues at length that one of ordinary skill, in attempting to apply the teachings of Hori figure 8 to another memory MISFET such as that of Nakazato et al., would not understand that the "MISFET for memory" gate structure, and the "MISFET for selection" gate structure would both have to overlie the region between a source and a drain (such as 2 and 3 of Hori). Examiner disagrees. The explicit teaching of figure 8 of Hori is precisely this. Moreover, one of ordinary skill would understand how the device of Hori figure 8 is supposed to work, and would not be

motivated to produce a device that does not work, as speculated by Applicant. More specifically, Applicant argues that there is "no suggestion for widening the distance" between source and drain regions of Nakazato to make room for the selection transistor of Hori. There is no reason why the distance between source and drain needs to be widened. One would simply form the "MISFET for memory" and the "MISFET for selection" between source and drain regions, exactly as suggested by figure 8 of Hori.

Applicant argues further with respect to claim 8 that including lightly-doped source and drain regions adjacent the heavily-doped source and drain regions would not give rise to the a structure having a region adjacent to the channel that is more lightly doped as compared to a second portion adjacent the channel. But that is precisely would lightly-doped source and drain regions are. They are lightly-doped regions, provided between the more heavily doped portions of the source and the drain, and the channel itself. If one provides lightly-doped source and drain regions as suggested by the examiner, each side of the channel would have a first lightly-doped region adjacent the channel, and a second, more heavily-doped region also adjacent the channel. (The word "adjacent" does not mean "in contact with," it simply means "nearby.")

Applicant argues with respect to claim 12 that there is no explicit teaching in the references that two transistors, one having a "MISFET for memory," and a second having a "MISFET for selection" as taught by Hori, would have different threshold voltages. Such transistors could not possibly have the same threshold voltages, however. In the "MISFET for selection," the voltage applied by the gate to the channel

is applied across a layer such as 17 in Hori figure 8. In the "MISFET for memory" the voltage is applied by the gate to the channel is applied across a layer such as 15, having exactly the same composition and thickness as layer 17, and in addition the voltage is applied across all of the layers lying above layer 15. The different structures means that there must be a difference in threshold voltages.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. Crane, whose telephone number is (571) 272-1652.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sara W. Crane
Primary Examiner
Art Unit 2811